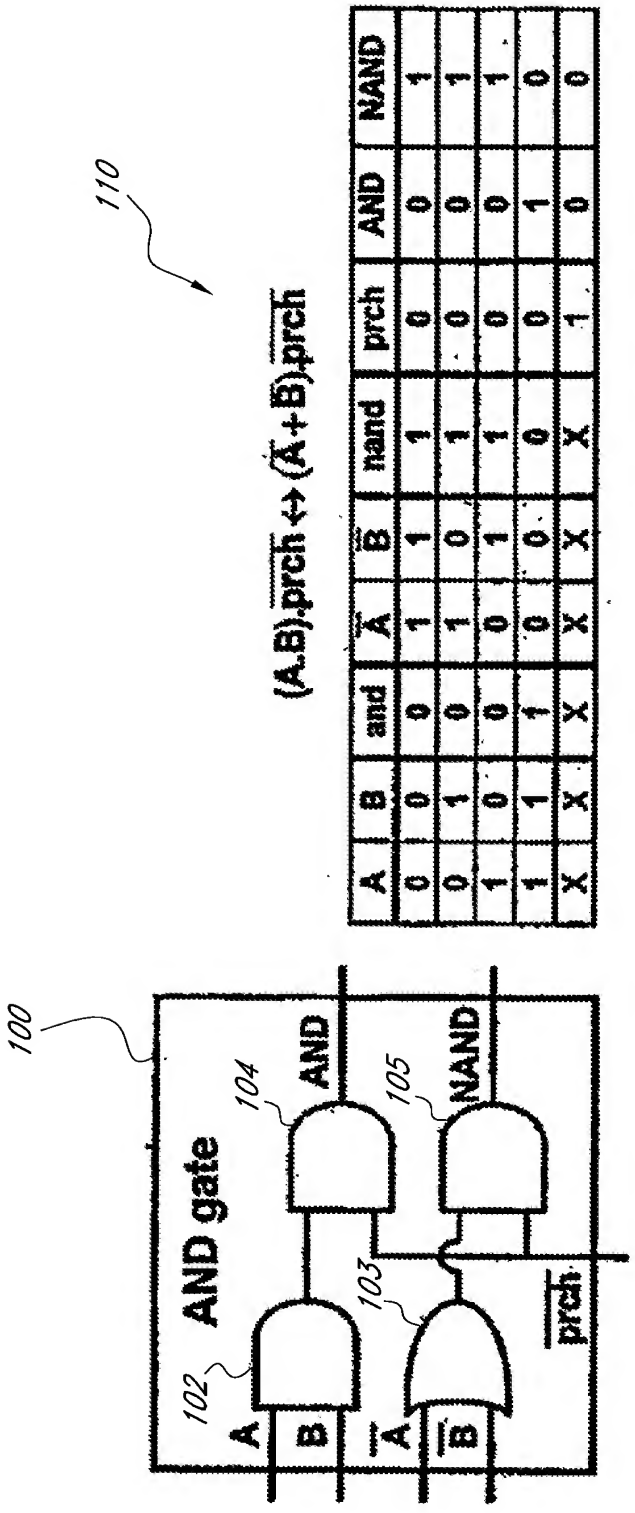

A	B	and	Ā	B̄	nand	prch	AND	NAND
0	0	0	1	1	1	0	0	1
0	1	0	1	0	1	0	0	1
1	0	0	0	1	1	0	0	1
1	1	1	0	0	0	0	1	0
X	X	X	X	X	X	1	0	0

FIG. 1

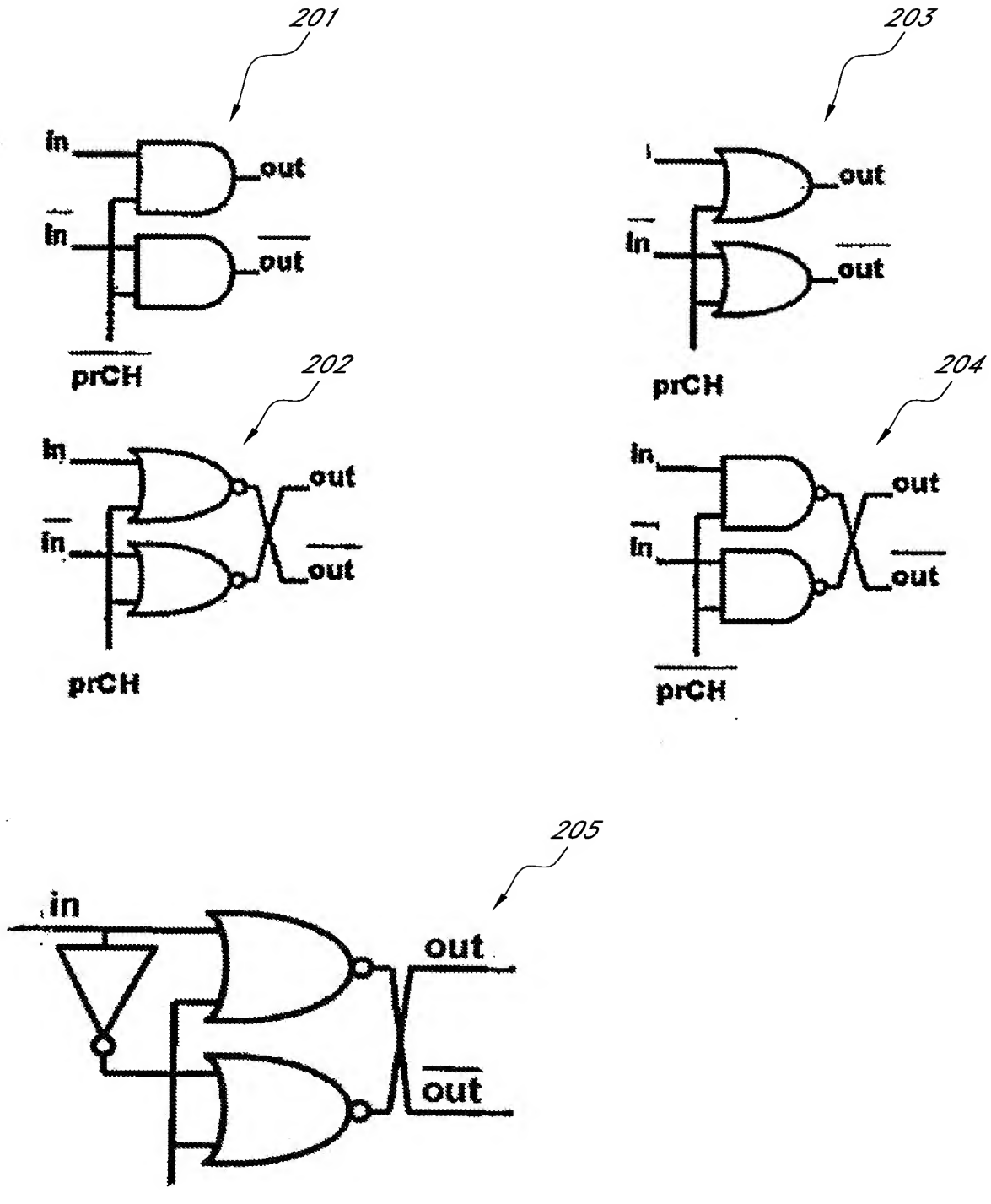
201
in
out
in
out
prCH
202
in
out
in
out
prCH
203
in
out
in
out
prCH
204
in
out
in
out
prCH
205
in
out
out

FIG. 2

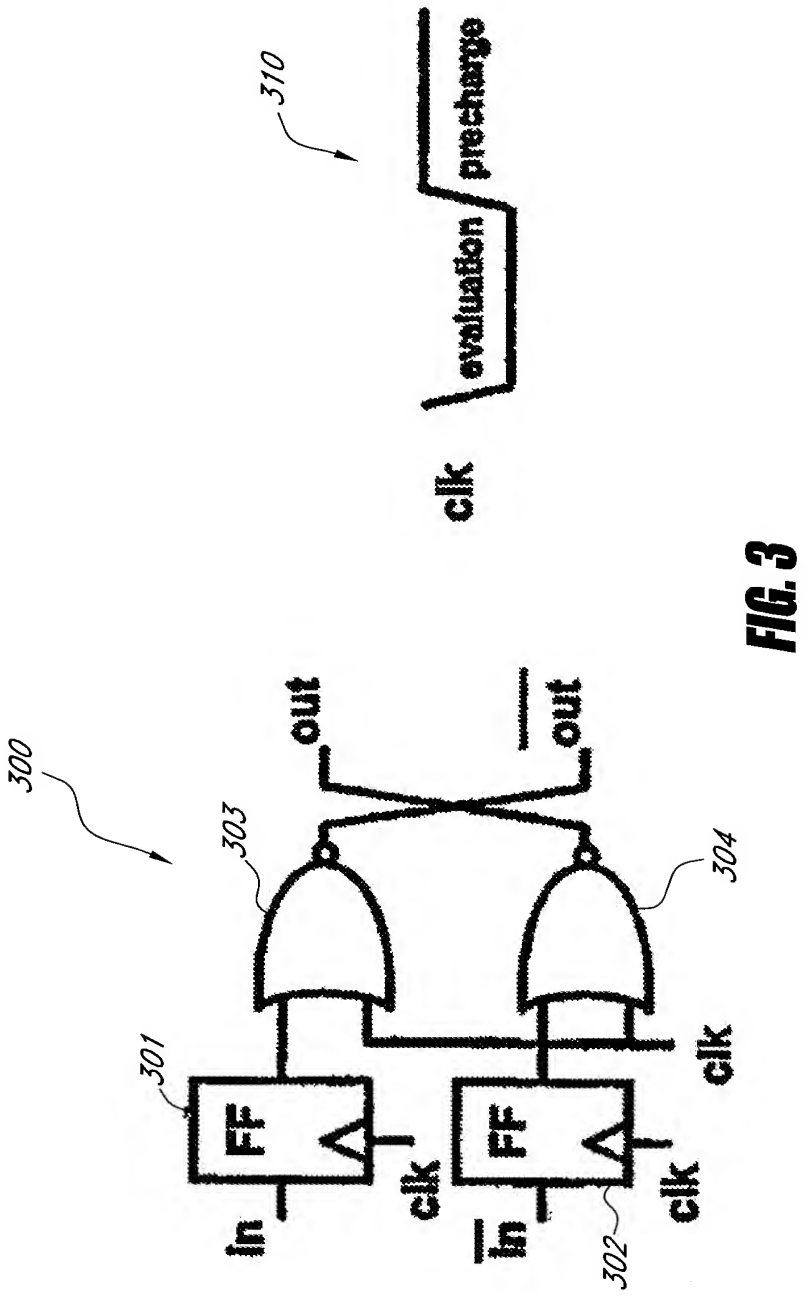
300
301
303
304
302
FF
FF
in
clk
in
clk
out
out
clk
clk
310
evaluation
precharge
clk

FIG. 3

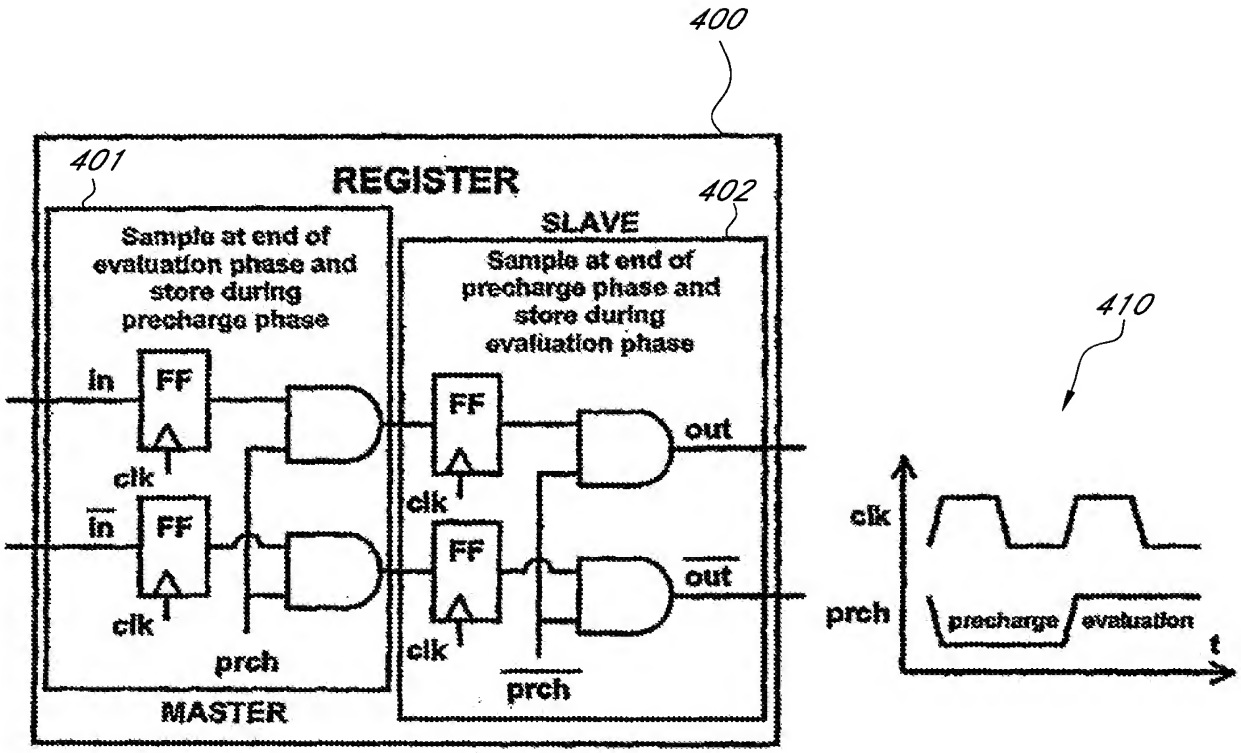
400
401
REGISTER
402
SLAVE
Sample at end of evaluation phase and store during precharge phase
Sample at end of precharge phase and store during evaluation phase
in
FF
clk
$\overline{in}$
FF
clk
prch
MASTER
FF
clk
out
FF
clk
$\overline{out}$
$\overline{prch}$
410
clk
prch
precharge
evaluation
t

FIG. 4

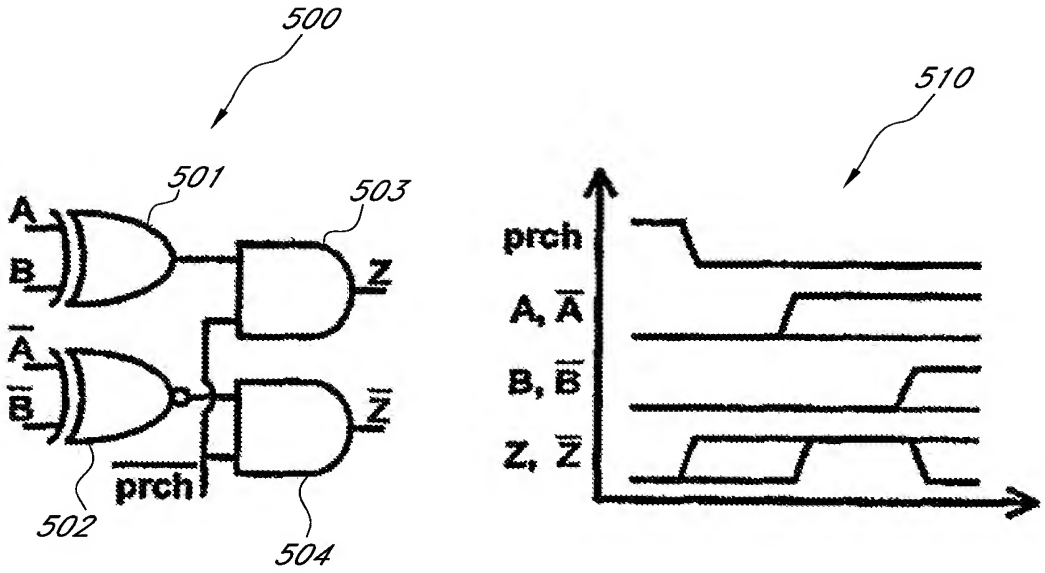
500
501
503
A
B
Z
$\bar{A}$
$\bar{B}$
$\bar{Z}$
prch
502
504
510
prch
A, $\bar{A}$
B, $\bar{B}$
Z, $\bar{Z}$

FIG. 5

610

A	B	and	$\overline{A}$	$\overline{B}$	nand	prch	AND	NAND
0	0	0	1	1	1	0	0	1
0	1	0	1	0	1	0	0	1
1	0	0	0	1	1	0	0	1
1	1	1	0	0	0	0	1	0
X	X	X	X	X	X	1	0	0

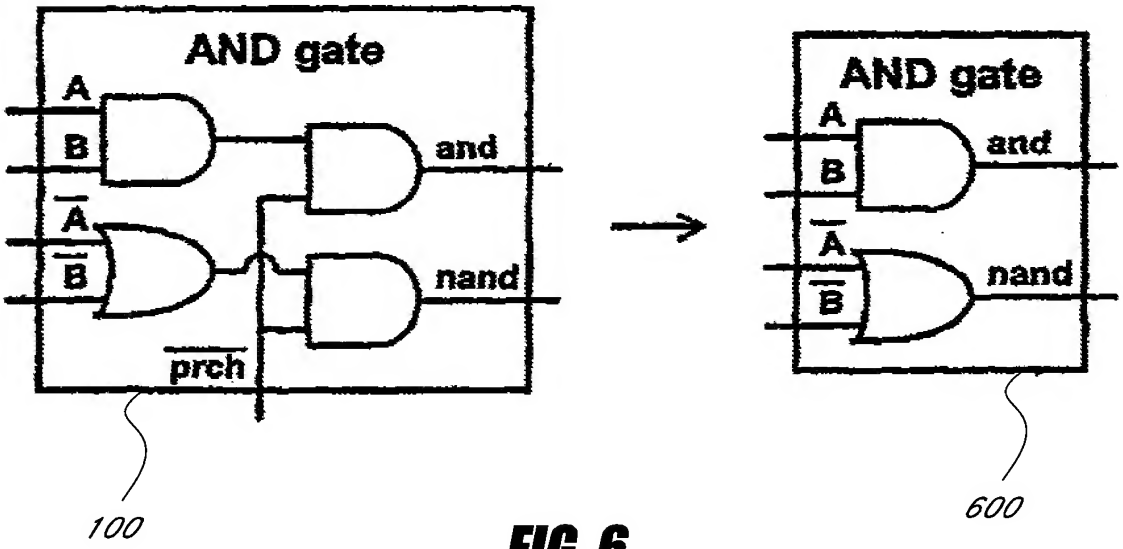

FIG. 6

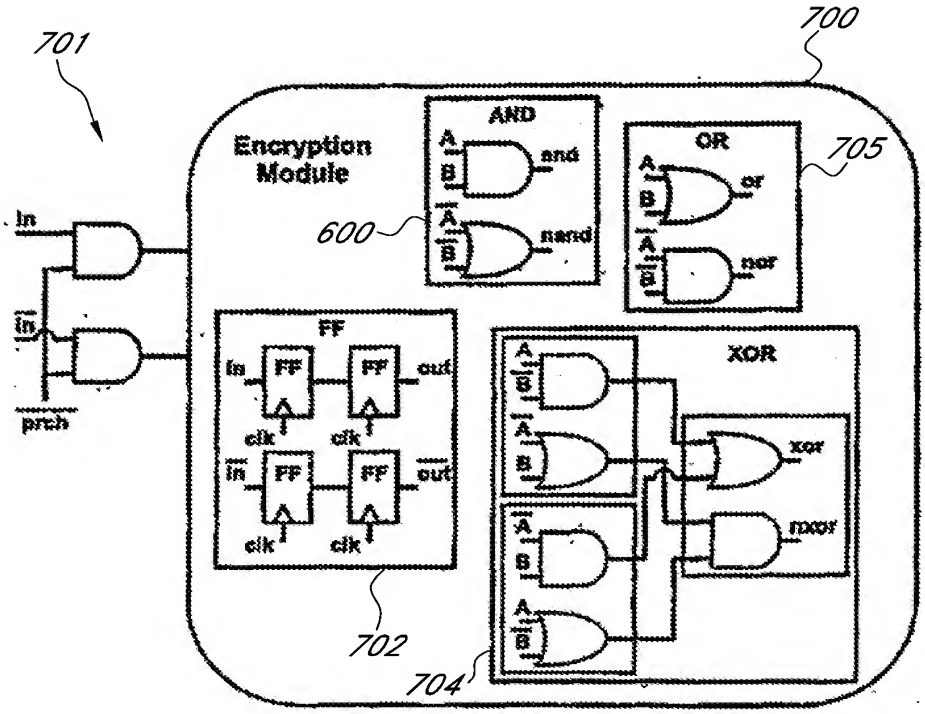
701
700
Encryption Module
AND
and
nand
600
OR
or
nor
705
FF
in
out
clk
XOR
xor
nxor
prch
702
704

FIG. 7

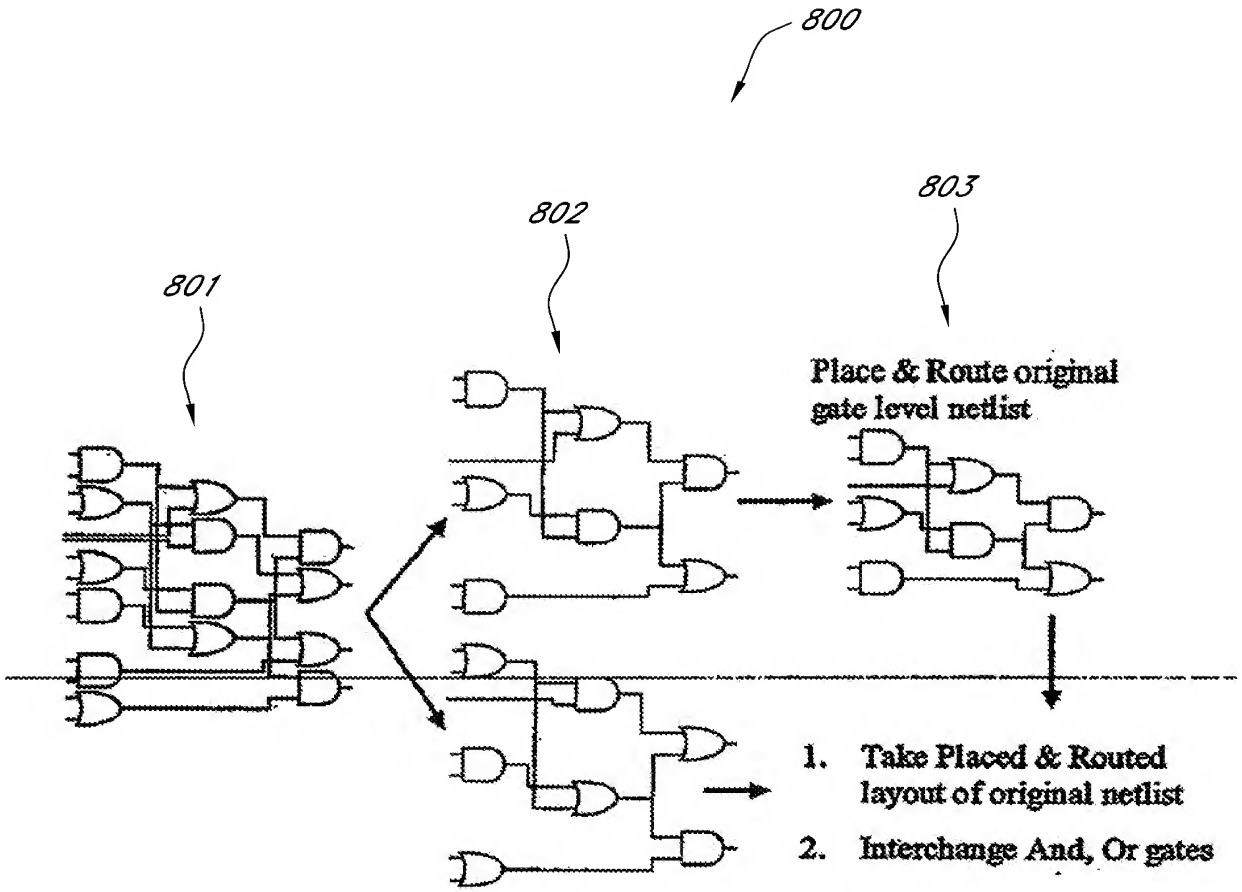
800
801
802
803
Place & Route original gate level netlist
1. Take Placed & Routed layout of original netlist
2. Interchange And, Or gates

FIG. 8

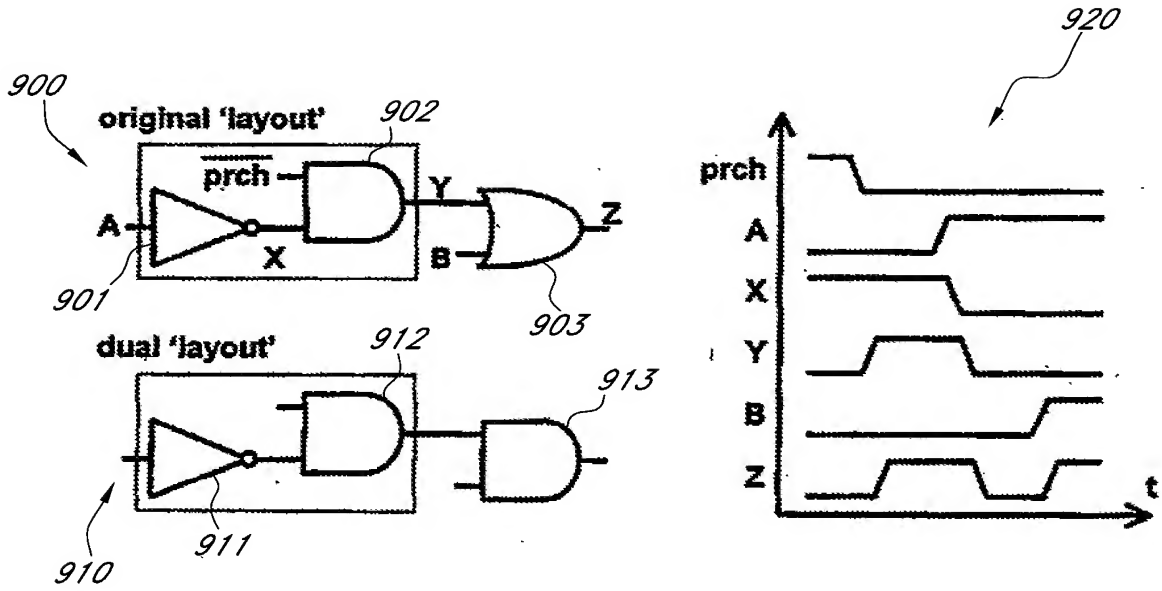
900
original 'layout'
902
prch
A
X
Y
B
Z
901
903
dual 'layout'
912
913
910
911
920
prch
A
X
Y
B
Z
t

FIG. 9

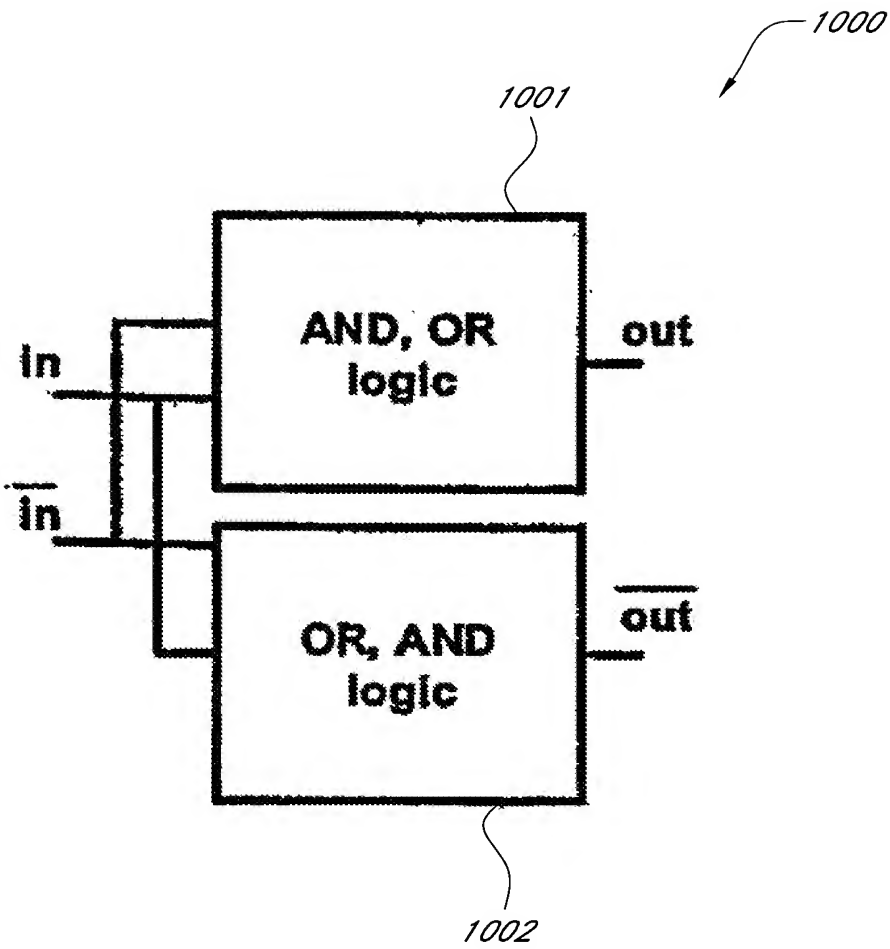
1000
1001
AND, OR
logic
in
$\overline{in}$
out
OR, AND
logic
$\overline{out}$
1002

FIG. 10

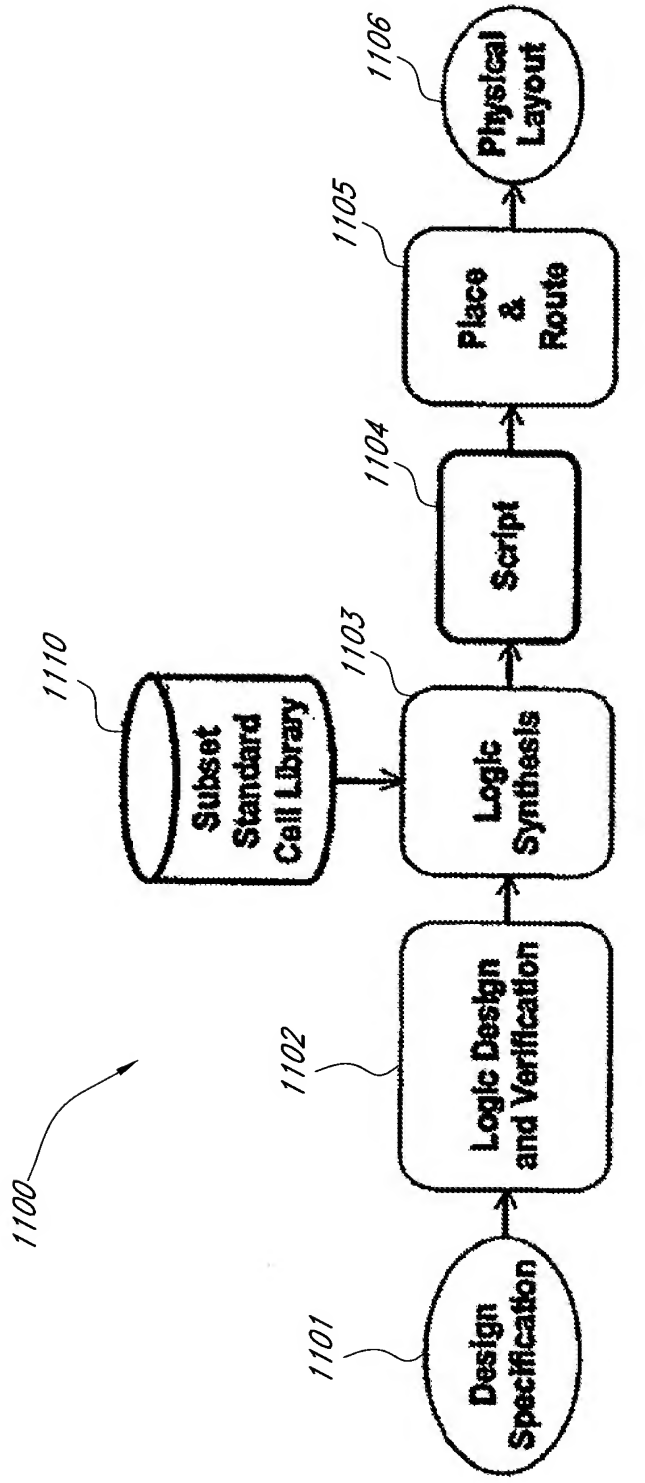
1100
1101
Design Specification
1102
Logic Design and Verification
1103
Logic Synthesis
1104
Script
1105
Place & Route
1106
Physical Layout
1110
Subset Standard Cell Library

FIG. 11

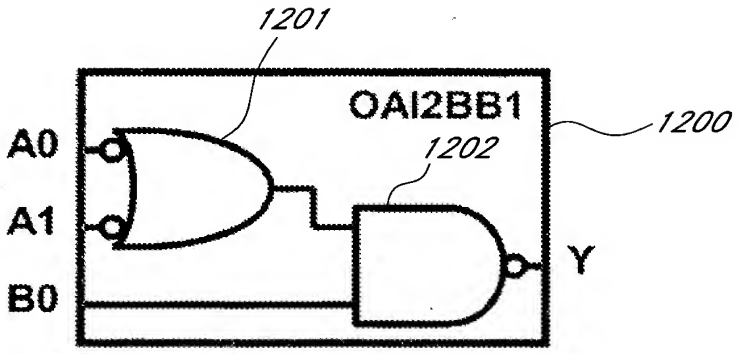

FIG. 12A

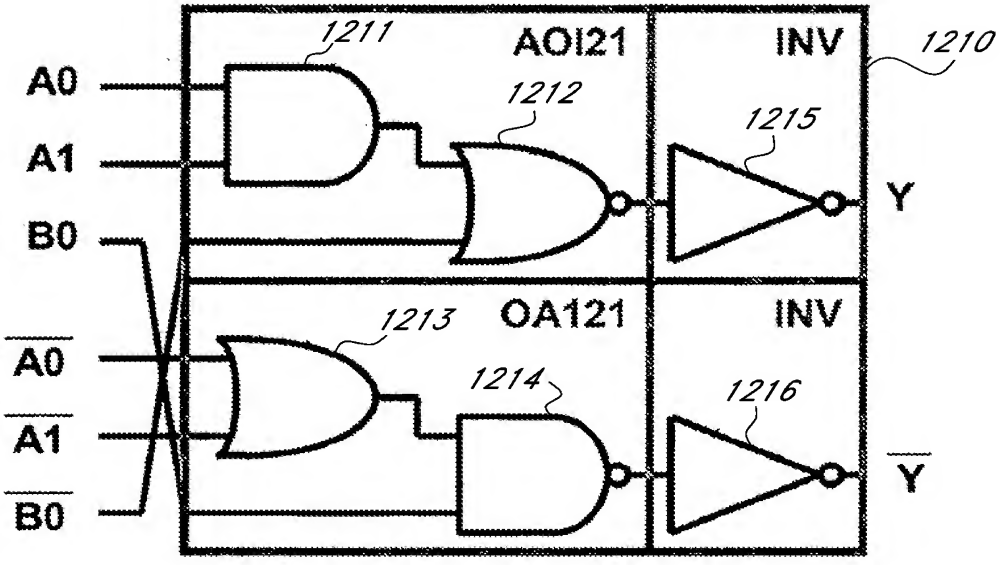

FIG. 12B

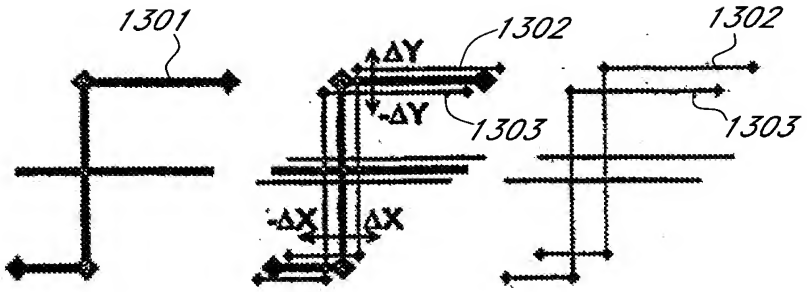

FIG. 13A **FIG. 13B** **FIG. 13C**

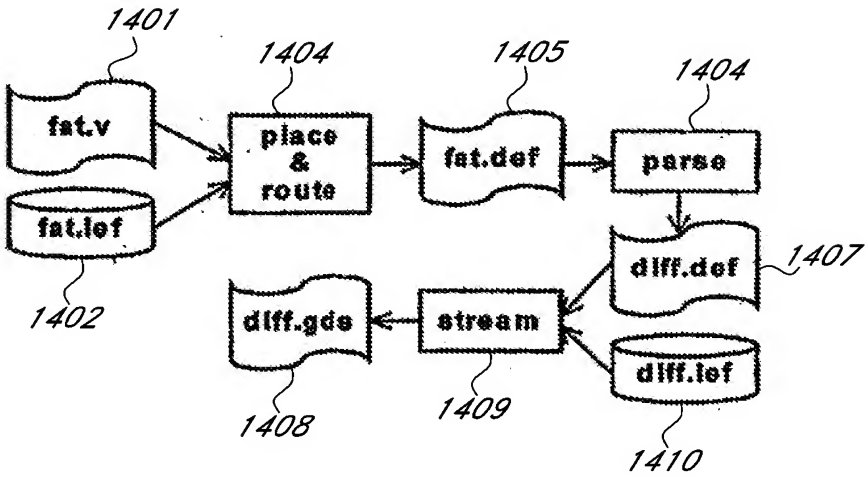

FIG. 14

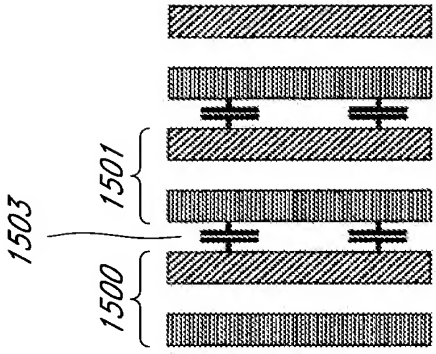

FIG. 15A

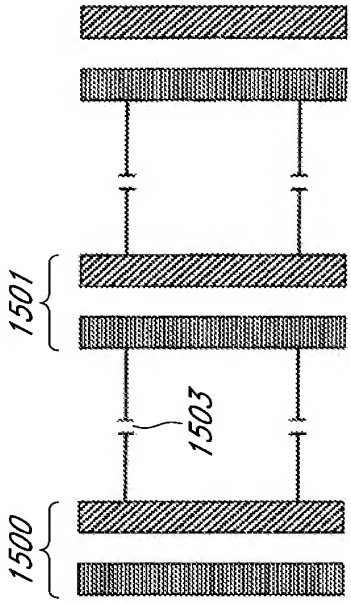

FIG. 15C

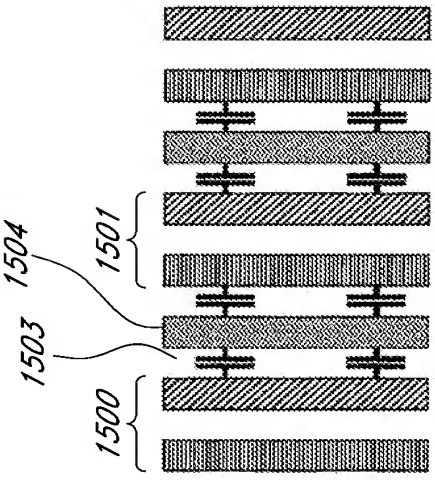

FIG. 15B